IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device comprising:

a plurality of memory circuits, each of ~~which~~ said plurality of memory circuits has a control circuit for sequentially controlling writing, and all of said plurality of memory circuits are provided on a single memory chip so as to share a data bus, and

a plurality of chip enable terminals for controlling the activity and inactivity of the memory circuits, respectively provided for each of the memory circuits; and

a master chip enable terminal for controlling the activity and inactivity of said single memory chip as a whole, the activity and inactivity of each of said memory circuits being controlled by a logical output of a signal of said master chip enable terminal and a respective chip enable terminal;

wherein each of said memory circuits is provided with a ready/busy signal terminal which corresponds to a respective chip enable terminal.

2.-3. (Canceled).

4. (Previously Presented): The electrically rewritable nonvolatile semiconductor memory device as set forth in claim 1, wherein said logical output is an output of an AND gate having the signal of said master chip enable terminal and the signal of a respective chip enable terminal as inputs.

5. (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device comprising:

a plurality of memory circuits, each of ~~which~~ said plurality of memory circuits has a control circuit for sequentially controlling writing, and all of said plurality of memory circuits are provided on a single memory chip so as to share a data bus,

wherein the activity and inactivity of each of the memory circuits are controlled by inputting a command, each of said plurality of memory circuits has a respective chip enable terminal, and a master chip enable terminal is provided for controlling the activity and inactivity of the single memory chip as a whole.

6. (Previously Presented): The electrically rewritable nonvolatile semiconductor memory device as set forth in claim 5, wherein a common chip enable terminal is provided for said plurality of memory circuits, and an enable signal inputted to said common chip enable terminal is supplied to a selected one of said memory circuits which has been selected by inputting said command.

7. (Canceled).

8. (Previously Presented): The electrically rewritable nonvolatile semiconductor memory device as set forth in claim 6, wherein a common ready/busy signal terminal is provided for said plurality of memory circuits, and a ready/busy state of said selected one of said memory circuits, which has been selected by inputting said command, is outputted to said common ready/busy signal terminal.

9. (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device comprising a plurality of memory circuits provided in a memory chip, each of said memory circuits including a corresponding at least one data buffer stage for ~~transmitting~~ storing writing data corresponding to an address, and wherein writing operations in said plurality of memory circuits are simultaneously carried out and a pass/fail result of each of said writing operations is output to each of said memory circuits and ~~stored~~ accumulated in the corresponding at least one data buffer stage.

10.-12. (Canceled).

13. (Currently Amended): An electrically rewritable nonvolatile semiconductor memory device comprising:

a plurality of memory circuits provided in a memory chip, each of said memory circuits including a corresponding at least one data buffer stage for transmitting writing data corresponding to an address, and wherein writing operations in said plurality of memory circuits are simultaneously carried out and a pass/fail result of each of said writing operations is output to each of said memory circuits;

wherein said electrically rewritable nonvolatile semiconductor has a mode whereby each of said plurality of memory circuits determines ~~it is determined~~ whether data is able to be inputted to said corresponding at least one data buffer stage by referring to [[said]] the memory circuit's corresponding pass/fail result, and a mode in which each of said plurality of memory circuits determines ~~it is determined~~ whether data is able to be input to said corresponding at least one data buffer stage without referring to said corresponding pass/fail result.

14. (Canceled).

15. (Previously Presented): The electrically erasable nonvolatile semiconductor of Claim 1, wherein each of said memory circuits has a stacked gate structure.

16. (Previously Presented): The electrically erasable nonvolatile semiconductor of Claim 9, wherein each of said memory circuits has a stacked gate structure.

17. (Previously Presented): The electrically erasable nonvolatile semiconductor of Claim 13, wherein each of said memory circuits has a stacked gate structure.

18. (Previously Presented): The electrically erasable nonvolatile semiconductor of Claim 15, wherein said stacked gate structure is a NAND structure.

19. (Previously Presented): The electrically erasable nonvolatile semiconductor of Claim 16, wherein said stacked gate structure is a NAND structure.

20. (Previously Presented): The electrically erasable nonvolatile semiconductor of Claim 17, wherein said stacked gate structure is a NAND structure.